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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,563	11/19/2001	Joseph C. Sher	MICRON.113C1	2553

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,563	SHER ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16, 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 09/29/06 has been entered. The rejections in previous office action are maintained.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javaniferd et al. (USP 5483486, Applicant submitted IDS) in view of Furumochi (USP 5473277, Applicant submitted IDS).

As to claim 1, Javanifrad et al. shows in figure 14 a circuit comprising: a reference circuit (316); a voltage regulator (318) electrically coupled to the reference circuit which generates a first control signal (REG); a charge pump (320) which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage (Vout). Thus, figure 14 shows all limitations of the claim except for the reference having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage

regulation devices. However, Furumochi's figure 5 shows a reference circuit having plurality of voltage regulation devices (T1-T4) and at least one bypass device (SW0) connected to at least one of the plurality of voltage regulation devices. Furumochi's circuit has the advantage of varying the voltage level at the output node (OUT). Thus, it would have been obvious to one having ordinary skill in the art to use Furumochi's figure for Javanifrad et al.'s reference circuit for the purpose of generating a variable reference voltage, therefore controlling the output level of the charge pump. Thus, with the combination, it is inherent that the at least one bypass device (SWO(TN4)) is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage, and the clamp circuit is configured to allow an output to vary below the clamping maximum (the total threshold of the diode connected transistors).

As to claim 2, Furumochi's figure 5 shows the plurality of voltage regulation devices comprise diodes.

As to claim 3, Furumochi's figure 5 shows the diodes are implemented through transistors.

As to claim 4, Furumochi's figure 5 further shows the bypass device comprising a fuse (FU) in series with a transistor (TN4).

As to claim 5, Furumochi's figure 5 shows bypass device is activated by blowing the fuse.

As to claim 6, with the combination of the prior arts, it is inherent that value of the operational supply voltage is reduced for each voltage regulation device bypassed.

As to claim 7, with the combination of the prior arts, it is inherent that the voltage regulation devices limit the maximum voltage output of the clamp circuit.

As to claim 8, with the combination of the prior arts, it is inherent that the first control signal reduces the test supply voltage when the voltage regulation devices limit the output of the clamp circuit.

As to claim 9, with the combination of the prior arts, it is inherent that the second control signal reduces the operational supply voltage when the non-bypassed voltage regulation devices (T1, T2..) limit the output of the clamp circuit.

Claims 10-16 and 25 recite similar limitations of claims 1-9. Therefore, they are rejected for the same reasons (see further in figure 4).

Response to Arguments

Furumochi's voltage clamp circuit is for only clamping voltage that is higher than the total threshold of the diode connected transistors. The clamp circuit can not clamp voltage that is lower than the total threshold of the diode connected transistors. Therefore, the clamp circuit would allow its output to vary below the clamping maximum or the total threshold of the transistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

October 31, 2006